CLAIMS

What is claimed is:

1. An electronic module comprising:
   an electrically conductive substrate;
   conductive feedthroughs in said conductive substrate;
   a multi-layer interconnection circuit having conductive traces fabricated on said conductive substrate;
   one or more integrated circuit chips having bumps that attach to selected traces of said interconnection circuits; and,
   wherein selected of said feedthroughs connect with selected traces of said interconnection circuits.
2. An electronic module comprising:
   an electrically conductive substrate;
   a multi-layer interconnection circuit having conductive traces fabricated on said conductive substrate;
   one or more integrated circuit chips having bumps that attach to selected traces of said interconnection circuits; and,
   one or more cables having bumps that attach to selected traces of said interconnection circuit.
3. The electronic module of claims 1 or 2 wherein one or more of said integrated circuit chips implement the function of a radio frequency transceiver.
4. The electronic module of claims 1 or 2 wherein said attachment of said bumps includes a well filled with solder interposed between each of said bumps and each of said traces.
5. An electronic system comprising:
   an electrically conductive substrate;
   a multi-layer interconnection circuit having conductive traces fabricated on said conductive substrate, selected traces of said interconnection circuits terminating at input/output pads; and,
   one or more electronic modules attached to said interconnection circuit using bumps that connect with said input/output pads.

6. The electronic module of claims 1-4 and including a top conductive plate bonded to the backsides of said integrated circuit chips.
7. The electronic system of claim 5 and including a top conductive plate bonded to the backsides of said modules.
8. The module or system of claims 1-7 wherein said conductive substrate is copper or dispersion strengthened copper.
9. The module of claim 6 or system of claim 7 wherein said top conductive plate is copper or dispersion strengthened copper.
10. The module of claim 1 wherein said multi-layer circuit comprises alternating layers of a patterned conductive material and a dielectric material.
11. The module of claim 10 wherein said dielectric is a thermoplastic material.
12. The module of claim 11 wherein said thermo plastic material is a liquid crystal polymer.
13. The module of claims 1-2 wherein said traces are formed from electroplated copper.
14. The module or system of claim 9 wherein said conductive top plate is replaced with a cooling chamber through which a cooling fluid may circulate.
15. The module or system of claims 1-5 wherein said bumps are gold stud bumps.
16. The module or system of claim 15 wherein said stud bumps are inserted into corresponding wells filled with solder provided in a special assembly layer on top of said interconnection circuits.
17. An electronic system fabricated on a blade comprising:
    a conductive blade substrate;
    a multi-layer interconnection circuit fabricated on said blade substrate, with selected traces terminating in input/output pads;
    a special assembly layer formed on top of said interconnection circuit that provides a well filled with solder at each of said input/output pads; and,
    a plurality of integrated circuit chips that are flip chip mounted using bumps that are inserted into said wells.
18. The blade system of claim 17 wherein said circuit chips are provided in groupings that include logic, memory, and communication functions.

19. The blade system of claim 18 wherein a plurality of said groups is arrayed to form a supergroup, and said supergroup may include an additional set of chips providing support functions for said supergroup.

20. The blade system of claim 19 including multiple supergroups, plus special chips for communicating between blades.

21. The blade system of claim 17 wherein said integrated circuit chips have their backsides thermally coupled to a conducting plate.

22. The blade system of claim 21 wherein said conducting plate is replaced with a flat chamber fabricated from thermally conducting material wherein said chamber is co-extensive with said blades and is filled with a cooling fluid that circulates within said chamber.

23. The blade system of claim 17 wherein said conductive substrate is copper or dispersion-strengthened copper.

24. The blade system of claim 17 wherein said imprintable dielectric material is a thermo plastic material.

25. The blade system of claim 17 wherein said thermo plastic material is a liquid crystal polymer.

26. The blade system of claim 17 wherein said traces are formed from electroplated copper.

27. The blade system of claim 17 wherein said bumps are gold stud bumps.

28. A method for fabricating a conductive plate with isolated feedthroughs comprising the steps of:

providing a suitable base material for said conductive plate such as copper, or an alloy of copper, or a dispersion hardened form of copper;

drilling said plate with holes on a suitable grid;

filling each of said holes with a plug of dielectric material and polishing to planarize;

drilling said dielectric plugs to create apertures concentric with said holes;

laminating a sheet of dielectric material so as to cover said apertures on one side of said conductive plate;

coating the side and bottom walls of said apertures with an adhesion layer such as titanium, followed by a seed layer of copper;

electroplating copper to fill said apertures and form feedthroughs;

polishing to planarize said electroplated copper and provide electrical isolation between said feedthroughs;

patterning a mask layer of material such as aluminum on said laminated dielectric material, with apertures matching said apertures in said dielectric plugs;

dry etching through said apertures to expose said electroplated copper;

depositing an adhesion layer of a material such as titanium and a seed layer of copper or gold onto said exposed electroplated copper; and,

electroplating said seed layer to produce a plated contact under each of said feedthroughs.

29. A dual damascene method for patterning a pair of layers including a conductive layer and a dielectric layer of an interconnection circuit comprising the steps of:

providing a planarized surface with exposed contact pads;

providing a layer of thermoplastic dielectric material over said planarized surface;

aligning a toolfoil and imprinting a dual level pattern, said dual levels including a lesser depth for trenches, and a greater depth for vias, with said vias aligned with said contact pads;

removing any remaining web of dielectric material to expose said contact pads;

coating said imprinted pattern with an adhesion layer of a material such as titanium followed by a seed layer of copper;

electroplating said seed layer to fill said vias and provide a suitable trench thickness of several microns; and,

polishing said electroplated material to provide a planarized surface and to provide electrical isolation between said trenches.

30. A method for imprinting a special assembly layer that includes a conductive well at each input/output pad of an interconnection circuit comprising the steps of:

providing exposed input/output pads at a polished and planarized surface;

providing a layer of thermoplastic material over said interconnection circuit;

aligning an embossing tool to alignment features of said interconnection circuit;

pressing said embossing tool into said imprintable dielectric to form a well including at least a portion of said well that is formed in close proximity to corresponding said input/output pad;

cooling to room temperature if necessary and separating said embossing tool from said

interconnection circuit;

removing by etching or other means a remaining web of said imprintable material if any, to expose said input output pads;

depositing a diffusion barrier material such as nickel to a thickness of approximately 1.5 microns;

polishing until a planarized surface is achieved and said wells are electrically isolated from one another; and,

filling said wells with solder paste.

31. A method for reworking defective die on a blade substrate comprising the steps of:

providing wells filled with solder at input/output pads of said blade substrate;

providing integrated circuits in bare die form;

providing conductive bumps at bonding sites of said integrated circuits, said bonding sites corresponding with said input/output pads;

assembling said integrated circuits onto said blade substrate by inserting said conductive bumps in said wells filled with solder, melting said solder as required;

providing means to test said blade substrate and identify any defective integrated circuits;

heating said blade substrate to a temperature below the solder melting point using a hot plate;

providing additional heat to said defective integrated circuit using hot inert gas applied to the backside of said bare die;

removing said defective integrated circuit by withdrawing said conductive bumps from said wells filled with solder;

cleaning the surface of said blade substrate around the site of said defective die as required;

providing additional solder in said wells as required; and,

inserting a good integrated circuit to replace said defective integrated circuit, providing heating to melt said solder and cooling as required.

32. A supercomputer arranged in the approximate shape of a cube comprising:

a parallel array of planar shaped cooling chambers;

blade components, each having a conductive substrate, wherein said substrate is thermally coupled to at least one of said cooling chambers and said blade components

each include more than 100 flip chip mounted integrated circuit chips assembled onto circuits fabricated on said substrate.

33. The supercomputer of claim 32 wherein said blades are interconnected using blade access cables attached to blade access ports provided on each of said blades.

34. The supercomputer of claim 33 wherein each of said blade access ports includes an array of terminals wherein each of said terminals comprises a well filled with solder, and said wells are spaced apart with a pitch of 200 microns or less.

35. A blade access cable comprising:

a rigid carrier for use during fabrication;

a release layer employing ultra violet release materials;

one or more signal layers;

two or more ground or power planes; and,

a stud bump at each input/output pad.

36. The blade access cable of claim 35 wherein said stud bumps are provided at a pitch of less than 200 microns.